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UM10018-01

ISP1160 PC Eval Kit User's Guide

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User's Guide

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Version	Date	Description	Author
1.0	Sep 2002	First version.	Jason Ong

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FIGURES

TABLES

1. Introduction

The ISP1160 is a single-chip Universal Serial Bus (USB) Host Controller (HC). It comes in two LQFP64 packages, each of which saves precious PCB space on your overall system design.

The ISP1160 is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, supporting data rates of 12 Mbit/s and 1.5 Mbit/s. Its target applications include embedded systems, portable devices and digital still cameras, among others.

The ISP1160 has two built-in downstream ports for the Host Controller. On each downstream port are overcurrent detection functions to monitor the current loading of the downstream port. If current conditions are abnormal, the ISP1160 has power switch controls to automatically disable the downstream port's current on the USB V_{BUS}. You may choose to ignore this function if you have no such demands in your design or have made your own design provisions.

The ISP1160 PC Evaluation Kit consists of the ISP1160 evaluation board and PC ISA interface card hardware as shown in Figure 1-1.

The ISP1160 evaluation board is a stand-alone evaluation board. However, when it is connected to the PC ISA interface card in the computer, it becomes a PC evaluation kit. You can then use the PC to perform evaluation testing. When the ISP1160 evaluation board is connected to a RISC processor interface card, it becomes a RISC processor evaluation kit. You can then use the RISC processor system to perform evaluation testing.

Figure 1-1: ISP1160 PC Evaluation Kit

2. Installation

To install the ISP1160 eval kit on a PC:

1. Plug the PC ISA interface card into the PC ISA slot.
2. Use a 40-way flat cable to connect the ISA interface card to the ISP1160 evaluation board. One end of the cable goes to connector J1001 on the ISA interface card, and the other to connector J1 on the ISP1160 evaluation board.
3. Check for correct jumper settings on the ISA interface card and the ISP1160 evaluation board.

The ISP1160 PC evaluation kit is ready for testing!

3. Jumper Settings

3.1. Default Jumper Settings

The next few pages show the default jumper settings. For settings that are not mentioned, leave them open.

3.1.1. For the PC ISA Interface Card

For JP1006, short pins 3-4 as shown in Figure 3-1. This will enable 16-bit data access.

The default setting for JP1005 is to short pins 3-4 (see Figure 3-2). This connects the ISP1160 DACK to the PC DACK6#.

Short pins 7-8 for JP1001, as shown in Figure 3-3. This connects the ISP1160 INT to PC IRQ10.

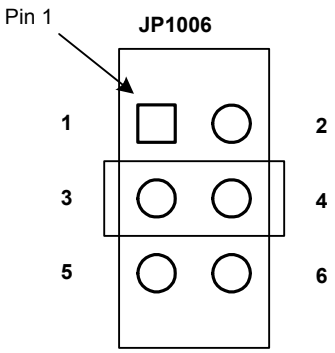


Figure 3-1: 16-Bit Access Enable Jumper

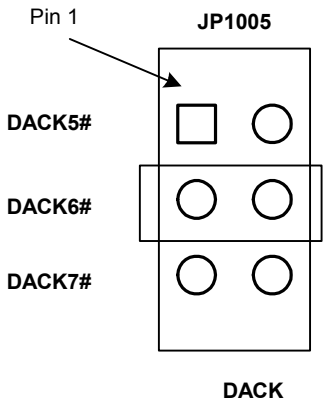


Figure 3-2: DACK Setting Jumper

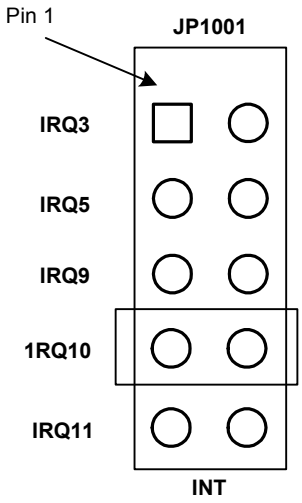


Figure 3-3: IRQ Setting Jumper

For JP1003, short pins 3-4 (see Figure 3-4). This connects the ISP1160 DREQ to the PC DREQ6.

For JP1007, short pins 3-4. This pulls SEL2-0 signals LOW. See Figure 3-5.

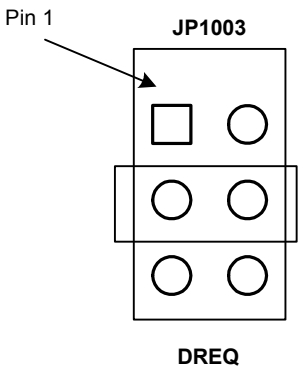


Figure 3-4: DREQ Setting Jumper

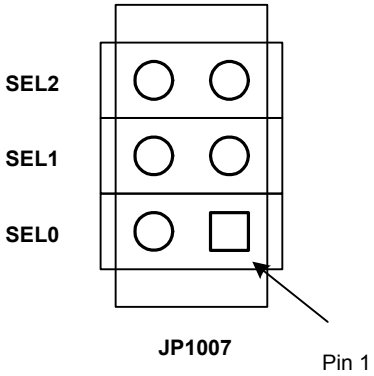


Figure 3-5: Select Jumper

Short pins 1-2 for JP1008. This shorts the $V_{CCLogic}$ signal to V_{CC} (see Figure 3-6).

For JP1010, short pins 1-2 as shown in Figure 3-7. This shorts V_{CC} to V_{CCPLD}.

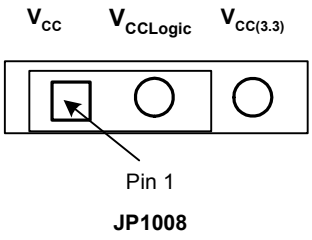


Figure 3-6: V_{CC} Jumper

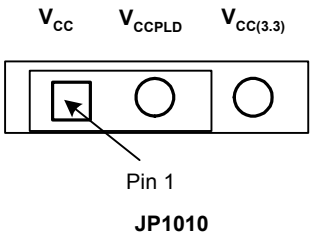


Figure 3-7: V_{CC} Jumper

3.1.2. For the ISP1160 Evaluation Board

For JP4, short pins 2-3 (see Figure 3-8). This connects the ISP1160 power supply V_{DD} to +5 V.

As given in Figure 3-9, short pins 1-2 for JP12. This restricts the ISP1160 hardware reset to the power-on reset only.

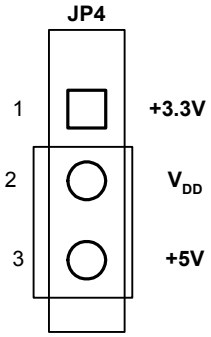


Figure 3-8: V_{DD} Input Select Jumper

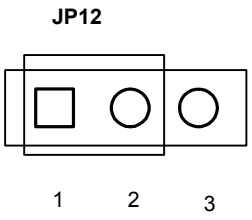


Figure 3-9: V_{CC} Jumper

For JP9 and JP10, short pins 3-4 as shown in Figure 3-10. This connects the ISP1160 overcurrent detection pins $\overline{H\_OC1}$ and $\overline{H\_OC2}$ to downstream port 1 VBUS_DN1 and downstream port 2 VBUS_DN2, respectively.

Note: The silkscreen for pins 2 and 3 of JP9 has been incorrectly swapped. The correct label for pin 2 and pin 3 must be H_PSW1 and H_OC1, respectively.

For JP5, short pins 1-2 as shown in Figure 3-11. This shorts pin 2 to the +5 V power supply.

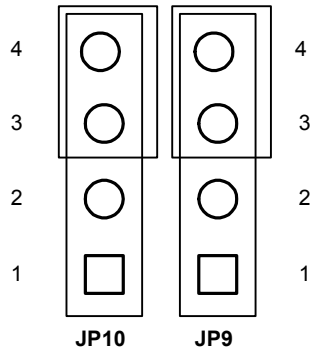


Figure 3-10: OC Input Select Jumpers

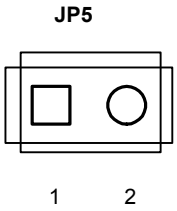


Figure 3-11: V_{BUS} Input Select Jumper

3.2. Jumper Summary

3.2.1. For the PC ISA Interface Card

Table 3-1: JP1001 IRQ Selection for the ISP1160 Host Controller Interrupt Requests

JP1001	ISP1160 Host Controller INT
Short pins 1-2	Connect to PC IRQ3
Short pins 3-4	Connect to PC IRQ5
Short pins 5-6	Connect to PC IRQ9
Short pins 7-8	Connect to PC IRQ10
Short pins 9-10	Connect to PC IRQ11

Table 3-2: JP1002 DREQ Channel Selection for the ISP1160 Host Controller DMA Request

JP1002	ISP1160 Host Controller DREQ	Remarks
Short pins 1-2	Connect to PC DREQ5	Must match with JP1004
Short pins 3-4	Connect to PC DREQ6	Must match with JP1004
Short pins 5-6	Connect to PC DREQ7	Must match with JP1004

Table 3-3: JP1004 DACK Channel Selection for the ISP1160 Host Controller DMA Acknowledge

JP1004	ISP1160 Host Controller DACK	Remarks
Short pins 1-2	Connect to PC DACK5#	Must match with JP1002
Short pins 3-4	Connect to PC DACK6#	Must match with JP1002
Short pins 5-6	Connect to PC DACK7#	Must match with JP1002

Table 3-4: JP1006 16-Bit I/O Access Enable and READY Enable

JP1006	Short	Open
Pins 1-2	Connect the ISP1160 READY signal to the PC IOCHRDY signal	Disconnect the ISP1160 READY signal with the PC IOCHRDY signal
Pins 3-4	Enable 16-bit I/O access	N/A
Pins 5-6	Reserved	

Table 3-5: JP1007 I/O Port Address Selection

SEL2, SEL1, SEL0	PC's Base I/O Address (Hex)	PC's I/O Address Range (Hex)
000	290	290 ~ 29F
001	300	300 ~ 30F
010	320	320 ~ 32F
011	360	360 ~ 36F
100	260	260 ~ 26F
101	220	220 ~ 22F
110	200	200 ~ 20F
111	340	340 ~ 34F

Table 3-6: JP1008 $V_{CCLogic}$ Settings

JP1008	$V_{CCLogic}$ Setting
Short pins 1-2	$V_{CCLogic}$ connected to V_{CC}
Short pins 2-3	$V_{CCLogic}$ connected to $V_{CC(3.3V)}$

Table 3-7: JP1009 A_D1 and A_D2 Settings

JP1009	A_D1 and A_D2 Settings
Short pins 1-2	A_D1 connected to SD1
Short pins 3-4	A_D2 connected to SD2

Table 3-8: JP1010 V_{CCPLD} Settings

JP1010	V_{CCPLD} Setting
Short pins 1-2	V_{CCPLD} connected to V_{CC}
Short pins 2-3	V_{CCPLD} connected to $V_{CC(3.3V)}$

3.2.2. For the ISP1160 Evaluation Board

Table 3-9: JP1 3.3 V Power Supply to the ISA Interface Board Selection

JP1	Select 3.3 V Power Supply to ISA Interface Board
Short	3.3 V supplied to ISA Interface Board
Open	3.3 V NOT supplied to ISA Interface Board

Table 3-10: JP2 Number of USB Downstream Ports Selection

JP2	Select Number of Host Controller Downstream Ports Available
Short	1 downstream port select
Open	2 downstream ports select

Table 3-11: JP3 ISP1160 V_{reg} Connection

JP3	V_{reg} Connected to +3.3 V
Short	Yes
Open	No

Table 3-12: JP4 ISP1160 V_{DD} Input Selection

JP4	ISP1160 V_{DD}
Short pins 1-2	Connect to +3.3 V
Short pins 2-3	Connect to +5 V

Table 3-13: JP5 5 V Power Supply to the ISA Interface Board Selection

JP5	Select 5 V Power Supply to the ISA Interface Board
Short	5 V supplied to the ISA Interface Board
Open	5 V NOT supplied to the ISA Interface Board

Table 3-14: JP6 V_{hold1} Selection

JP6	Select 3.3 V Power Supply to V_{hold1}
Short	3.3 V connected to V_{hold1}
Open	3.3 V NOT connected to V_{hold1}

Table 3-15: JP7 V_{hold2} Selection

JP7	Select 3.3 V Power Supply to V_{hold2}
Short	3.3 V connected to V_{hold2}
Open	3.3 V NOT connected to V_{hold2}

Table 3-16: JP8 Downstream Port V_{BUS} Input Selection

JP8	Downstream Port V_{BUS} Input
Short pins 1-2	+5 V comes from the USB upstream port
Short pins 2-3	+5 V comes from the on-board regulator output

Table 3-17: JP9 and JP10 Downstream Ports' Overcurrent Detection Input Selection

	JP9
Open pins 1-2	Enable power switch control for the downstream port 1
Short pins 1-2	Disable power switch control for the downstream port 1
Open pins 3-4	Disable downstream port 1 the OC detection
Short pins 3-4	Enable downstream port 1 the OC detection

Table 3-18: JP11 On-Board Regulator Selection

JP11	Select On-Board Regulator
Short	V_{DD} is connected to the on-board regulator
Open	V_{DD} is NOT connected to the on-board regulator

Table 3-19: JP12 Reset Input Selection

JP12	Reset Input Select
Short pins 1-2	Reset by mechanical switch
Short pins 2-3	Hardware reset by power-on only

4. PC Resources Assignment

4.1. I/O Address Assignment

I/O address assignment is shown in Table 4-1.

Table 4-1: I/O Address Assignment for the ISP1160

I/O Port Base Address (Hex)	Description	Remarks
290	Host Controller **data** port; **16-bit** access; **Read/Write**	—
292	Host Controller **command** port; **16-bit** access; **Write** only	—

4.2. IRQ Assignment

The ISP1160 Host Controller interrupt request output INT can be connected to PC IRQ3, IRQ5, IRQ9, IRQ10 and IRQ11. This is selectable by setting jumper JP1001 pins 1-2, 3-4, 5-6, 7-8 and 9-10, respectively.

4.3. DMA Channel Assignment

Three 16-bit DMA channels can be used: 5, 6 and 7. Each DMA operation for the ISP1160 can be set to one of these three DMA channels.

For the Host Controller, the DMA request output DREQ1 can be connected to PC DREQ5, DREQ6 or DREQ7 by setting jumper JP1002 pins 1-2, 3-4 or 5-6, respectively. The DMA acknowledge input DACK can be connected to PC DACK5#, DACK6# or DACK7# by setting jumper JP1004 pins 1-2, 3-4 or 5-6, respectively.

5. Power Supply and LED Indicators

The ISP1160 PC evaluation kit's power supply input comes from the PC ISA bus's +5 V. Therefore, there is no need for any other external power supply input.

The power supply input connectors—J8 for +5 V, and J9 for +3.3 V—on the evaluation board are reserved for the use of other RISC processor evaluation kits. Therefore, make sure you do not connect any power supply input to these connectors.

There are some LEDs on board to indicate the status of power supply. On the PC ISA interface card, DS1003 is the +5 V indicator. On the ISP1160 evaluation board, DS1 is the +5 V indicator and DS2 is the +3.3 V indicator.

6. Connectors' Pin Signal Information

6.1. For the PC ISA Interface Card

The 16-bit interface connector J1001 pin diagram is shown in Figure 6-1. This connector will be connected to the ISP1160 evaluation board connector J1 via a 40-way cable. Table 6-1 describes pin signals.

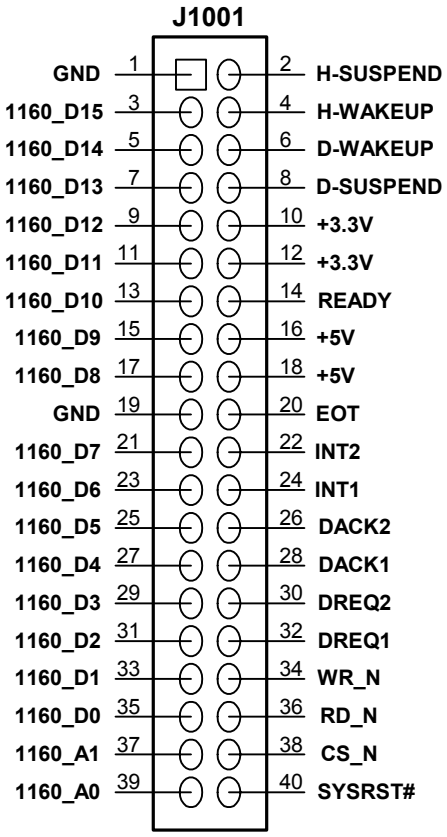


Figure 6-1: 16-Bit Interface Connector

Table 6-1: 16-Bit Interface Connector Pins Signal Description

Pin No.	Signal Name	Description	Remarks
3, 5, 7, 9, 11, 13, 15, 17, 21, 23, 25, 27, 29, 31, 33, 35	1160_D[15:0]	ISP1160 data bus	—
1, 19	GND	Ground	—
37, 39	1160_A[1:0]	ISP1160 address lines	—
2	H_SUSPEND	ISP1160 pin signal H_SUSPEND	—
4	H_WAKEUP	ISP1160 pin signal H_WAKEUP	—
10, 12	+3.3 V	Evaluation board power supply +3.3 V	—
16, 18	+5 V	ISA bus power supply +5 V	—
20	EOT	ISP1160 pin signal EOT	—
24	INT1	ISP1160 pin signal INT	—
28	DACK1	ISP1160 pin signal DACK	—
32	DREQ1	ISP1160 pin signal DREQ	—
34	$\overline{WR}$	ISP1160 pin signal $\overline{WR}$	—
36	$\overline{RD}$	ISP1160 pin signal $\overline{RD}$	—
38	$\overline{CS}$	ISP1160 pin signal $\overline{CS}$	—
40	SYSRST#	Reset signal comes from PC	Same as $\overline{SYS\_RST}$ on the evaluation board

The J1003 connector given in Figure 6-2 is used to test ISA signals. The pin signals are described in Table 6-2.

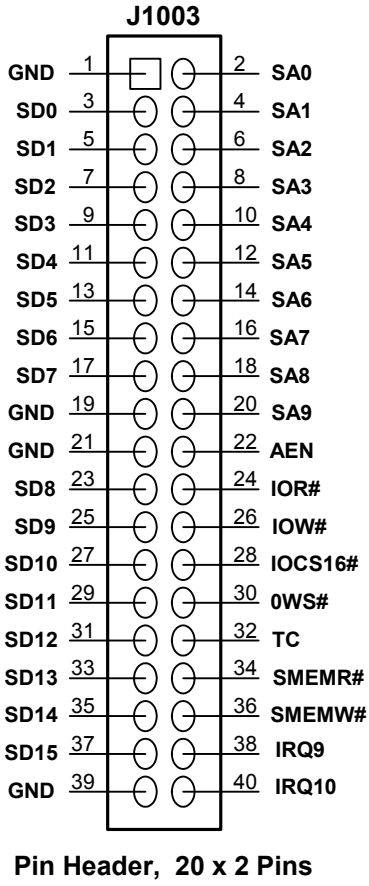


Figure 6-2: Testing Points Connector for ISA Signals

Table 6-2: Testing Points Connector for ISA Signals

Pin No.	Signal Name	Description	Remarks
1, 19, 21, 39	GND	Ground	—
3, 5, 7, 9, 11, 13, 15, 17, 23, 25, 27, 29, 31, 33, 35, 37	SD[15:0]	PC ISA data bus	—
2, 4, 6, 8, 10, 12, 14, 16, 18, 20	SA[9:0]	PC ISA address bus	—
22	AEN	PC ISA bus signal AEN	—
24	IOR#	PC ISA bus signal IOR#	—
26	IOW#	PC ISA bus signal IOW#	—
28	IOCS16#	PC ISA bus signal IOCS16#	—
30	0WS#	PC ISA bus signal 0WS#	—
32	TC	PC ISA bus signal TC	—
34	SMEMR#	PC ISA bus signal SMEMR#	—
36	SMEMW#	PC ISA bus signal SMEMW#	—
38	IRQ9	Interrupt Request 9	—
40	IRQ10	Interrupt Request 10	—

6.2. For the ISP1160 Evaluation Board

The pin assignment on the 16-bit interface connector J1 is the same as the ISA interface card connector J1001. For pin assignments and pin description, see Figure 6-1 and Table 6-1, respectively.

Connectors J2 and J3 are for debugging. See Figure 6-3 for pin assignment and Table 6-3 and Table 6-4 for pin description.

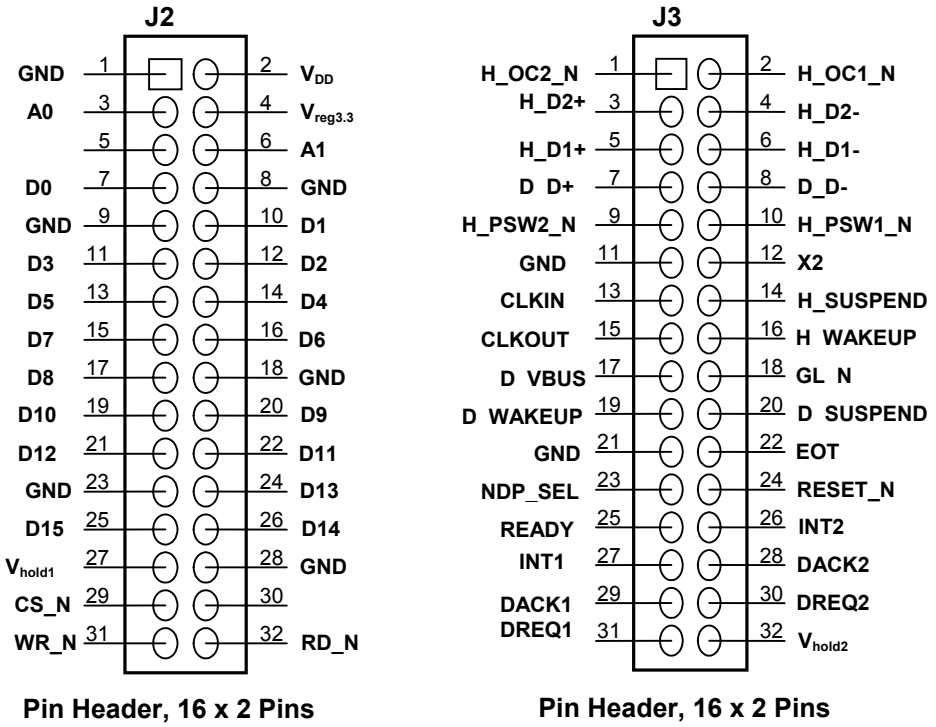


Figure 6-3: J2 and J3 Connector for Debugging of Evaluation Board Signals

Table 6-3: Pin Description for the J2 Connector

Pin No.	Signal Name	Description	Remarks
1, 8, 9, 18, 23, 28	GND	Ground	—
7, 10-17, 19-22, 24-26	D[15:0]	Evaluation board data bus	—
3, 6	A[1:0]	Evaluation board address bus	—
2	V_{DD}	V_{DD} power supply	—
4	$V_{reg(3.3)}$	+3.3 V power supply from regulator	—
27	V_{hold}	Voltage holding power supply	—
29	$\overline{CS}$	Active LOW chip select	—
31	$\overline{WR}$	Active LOW write	—
32	$\overline{RD}$	Active LOW read	—

Table 6-4: Pin Description for the J3 Connector

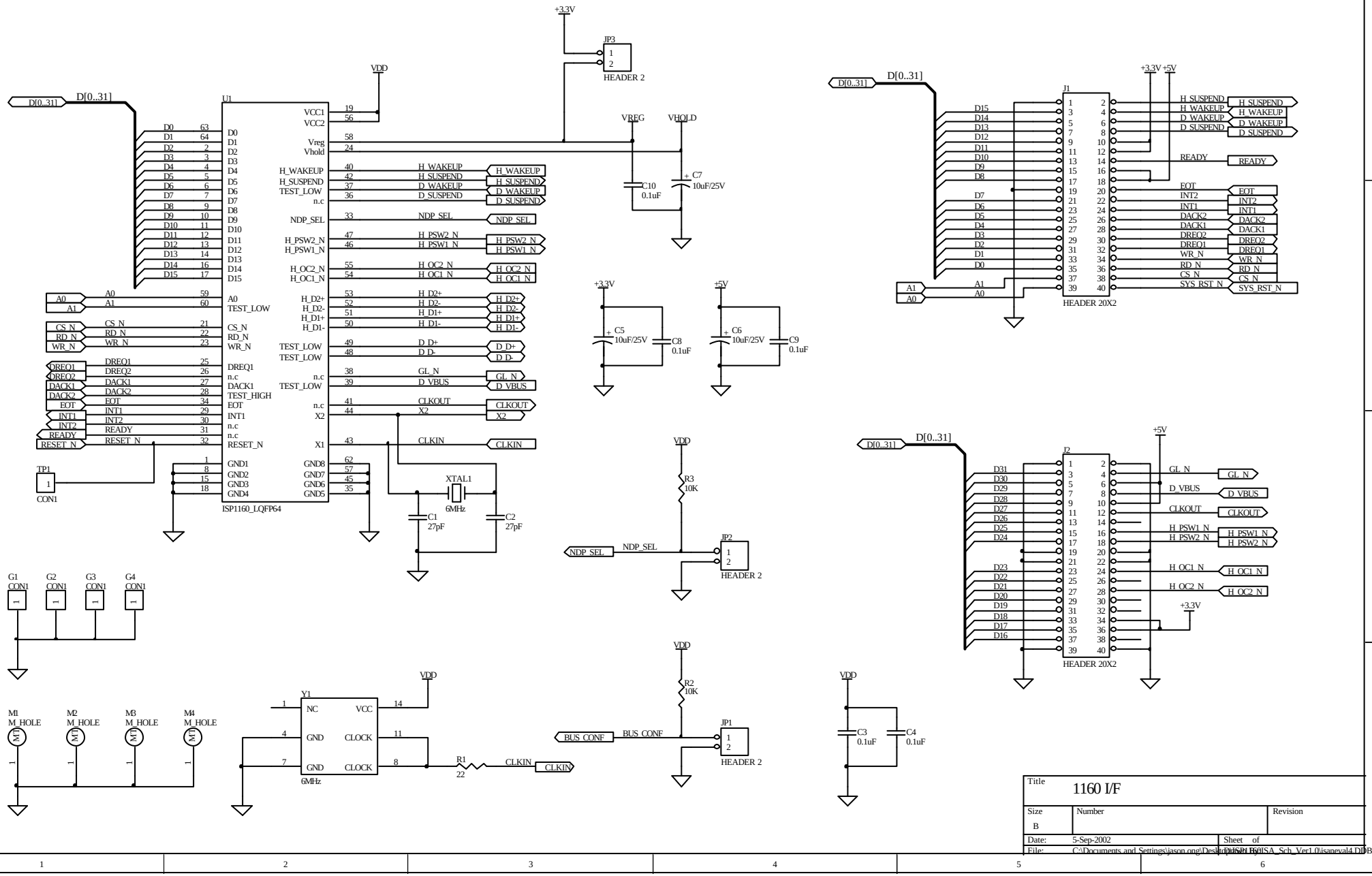
Pin No.	Signal Name	Description	Remarks
11, 21	GND	Ground	—
1	$\overline{H\_OC2}$	Overcurrent sense for downstream port 2	—
2	$\overline{H\_OC1}$	Overcurrent sense for downstream port 1	—
3	H_D2+	D+ for downstream port 2	—

Pin No.	Signal Name	Description	Remarks
4	H_D2-	D- for downstream port 2	—
5	H_D1+	D+ for downstream port 1	—
6	H_D1-	D- for downstream port 1	—
9	$\overline{\text{H\_PSW2}}$	Power switch control for downstream port 2	—
10	$\overline{\text{H\_PSW1}}$	Power switch control for downstream port 1	—
12	X2	Crystal Output	—
13	CLKIN	Crystal Input	—
14	H_SUSPEND	Host Controller suspend output	—
15	CLKOUT	Programmable Clock Output	—
16	H_WAKEUP	Host Controller wakeup input	—
22	EOT	End of DMA transfer	—
23	NDP_SEL	Number of downstream port select	—
24	$\overline{\text{RESET}}$	Active LOW reset input	—
27	INT1	Host Controller Interrupt Request Output	—
29	DACK1	Host Controller DMA Acknowledge	—
31	DREQ1	Host Controller DMA Request Output	—
32	V_{hold2}	Voltage hold power supply	—

7. USB Ports

Connector **J5** is for the USB **downstream port 1** and connector **J6** is for the USB **downstream port 2**.

Appendix A. Schematics


+3.3V
JP3
HEADER 2
VDD
D[0..31]
U1
VCC1
VCC2
Vreg
Vhold
VREG
VHOLD
C10
0.1uF
C7
10uF/25V
H_WAKEUP
H_SUSPEND
TEST_LOW
NDP_SEL
H_PSW2_N
H_PSW1_N
H_OC2_N
H_OC1_N
H_D2+
H_D2-
H_D1+
H_D1-
D_D+
D_D-
GL_N
D_VBUS
CLKOUT
X2
X1
CLKIN
A0
A1
CS_N
RD_N
WR_N
DREQ1
DREQ2
DACK1
DACK2
EOT
INT1
INT2
READY
RESET_N
TEST_HIGH
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
ISP1160_LQFP64
TP1
CON1
XTAL1
6MHz
C1
27pF
C2
27pF
C5
10uF/25V
C8
0.1uF
C6
10uF/25V
C9
0.1uF
+5V
R3
10K
JP2
HEADER 2
G1
G2
G3
G4
M1
M2
M3
M4
M_HOLE
Y1
NC
VCC
GND
CLOCK
R1
22
R2
10K
JP1
BUS_CONF
C3
0.1uF
C4
0.1uF
J1
HEADER 20X2
READY
EOT
INT2
INT1
DACK2
DACK1
DREQ2
DREQ1
WR_N
RD_N
CS_N
SYS_RST_N
J2
D_VBUS
CLKOUT
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H_PSW2_N
H_OC1_N
H_OC2_N
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Size
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File:
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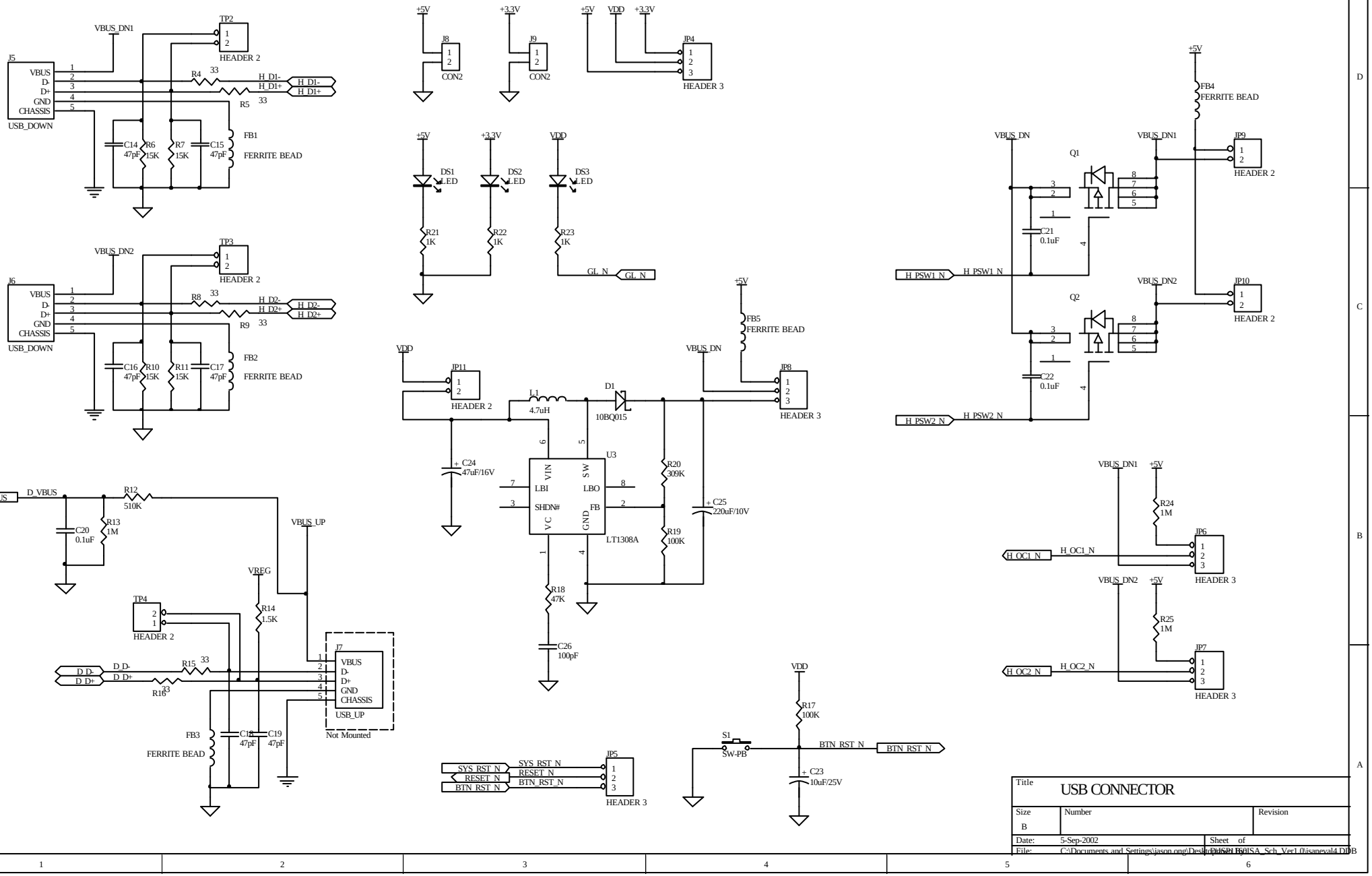

Title	USB CONNECTOR
Size	B
Number	
Revision	
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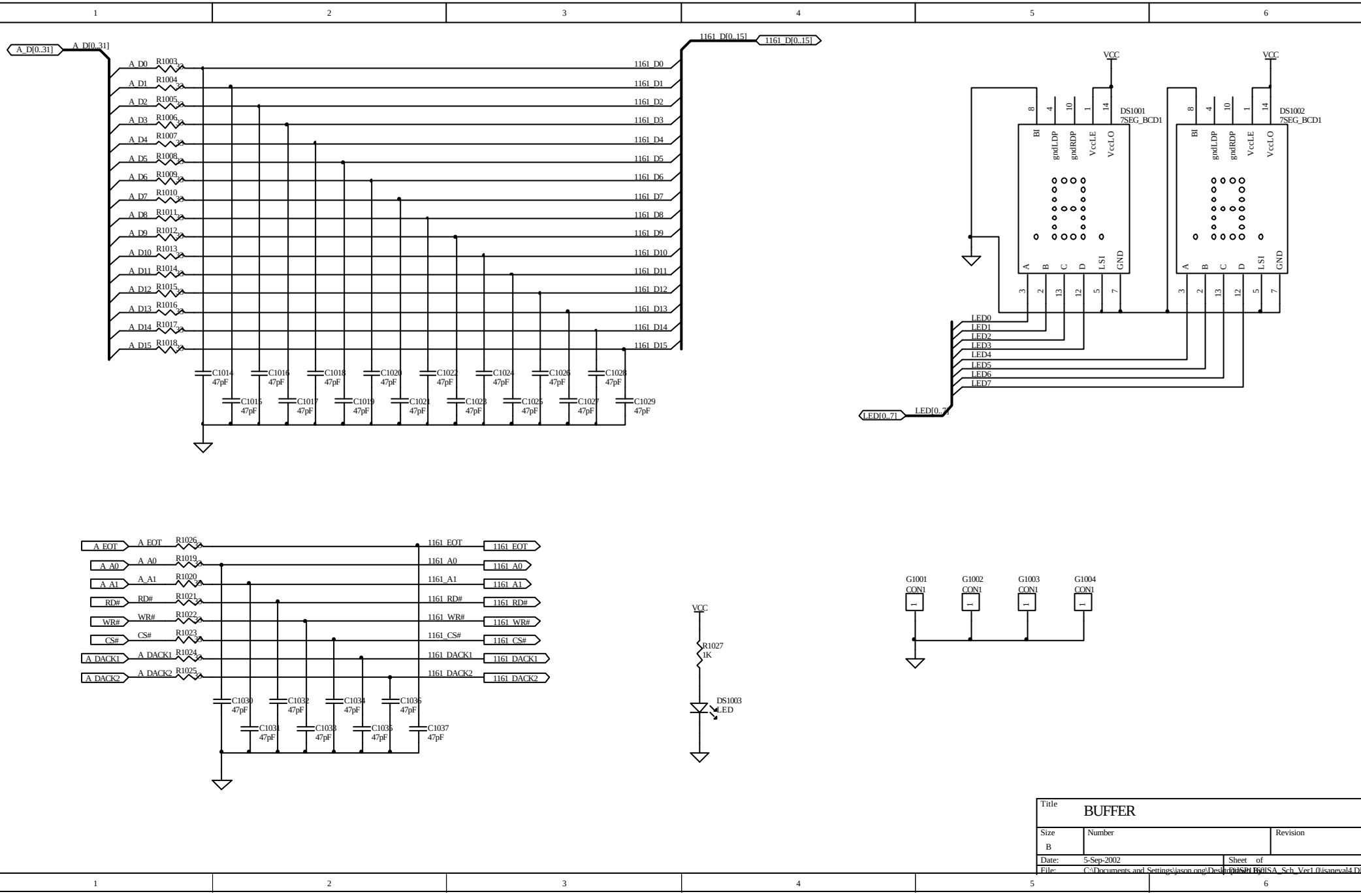
Drawn By:	


A_D[0..31]
A_D[0..31]
A_D0
A_D1
A_D2
A_D3
A_D4
A_D5
A_D6
A_D7
A_D8
A_D9
A_D10
A_D11
A_D12
A_D13
A_D14
A_D15
R1003
R1004
R1005
R1006
R1007
R1008
R1009
R1010
R1011
R1012
R1013
R1014
R1015
R1016
R1017
R1018
1161_D0
1161_D1
1161_D2
1161_D3
1161_D4
1161_D5
1161_D6
1161_D7
1161_D8
1161_D9
1161_D10
1161_D11
1161_D12
1161_D13
1161_D14
1161_D15
1161_D[0..15]
1161_D[0..15]
C1014 47pF
C1015 47pF
C1016 47pF
C1017 47pF
C1018 47pF
C1019 47pF
C1020 47pF
C1021 47pF
C1022 47pF
C1023 47pF
C1024 47pF
C1025 47pF
C1026 47pF
C1027 47pF
C1028 47pF
C1029 47pF
VCC
VCC
DS1001
7SEG_BCD1
DS1002
7SEG_BCD1
Bl
gndLDP
gndRDP
VccLE
VccLO
A
B
C
D
LSI
GND
LED0
LED1
LED2
LED3
LED4
LED5
LED6
LED7
LED[0..7]
LED[0..7]
A_EOT
A_A0
A_A1
RD#
WR#
CS#
A_DACK1
A_DACK2
R1026
R1019
R1020
R1021
R1022
R1023
R1024
R1025
1161_EOT
1161_A0
1161_A1
1161_RD#
1161_WR#
1161_CS#
1161_DACK1
1161_DACK2
C1030 47pF
C1031 47pF
C1032 47pF
C1033 47pF
C1034 47pF
C1035 47pF
C1036 47pF
C1037 47pF
VCC
R1027
1K
DS1003
LED
G1001
G1002
G1003
G1004
CON1
Title
BUFFER
Size
B
Number
Revision
Date:
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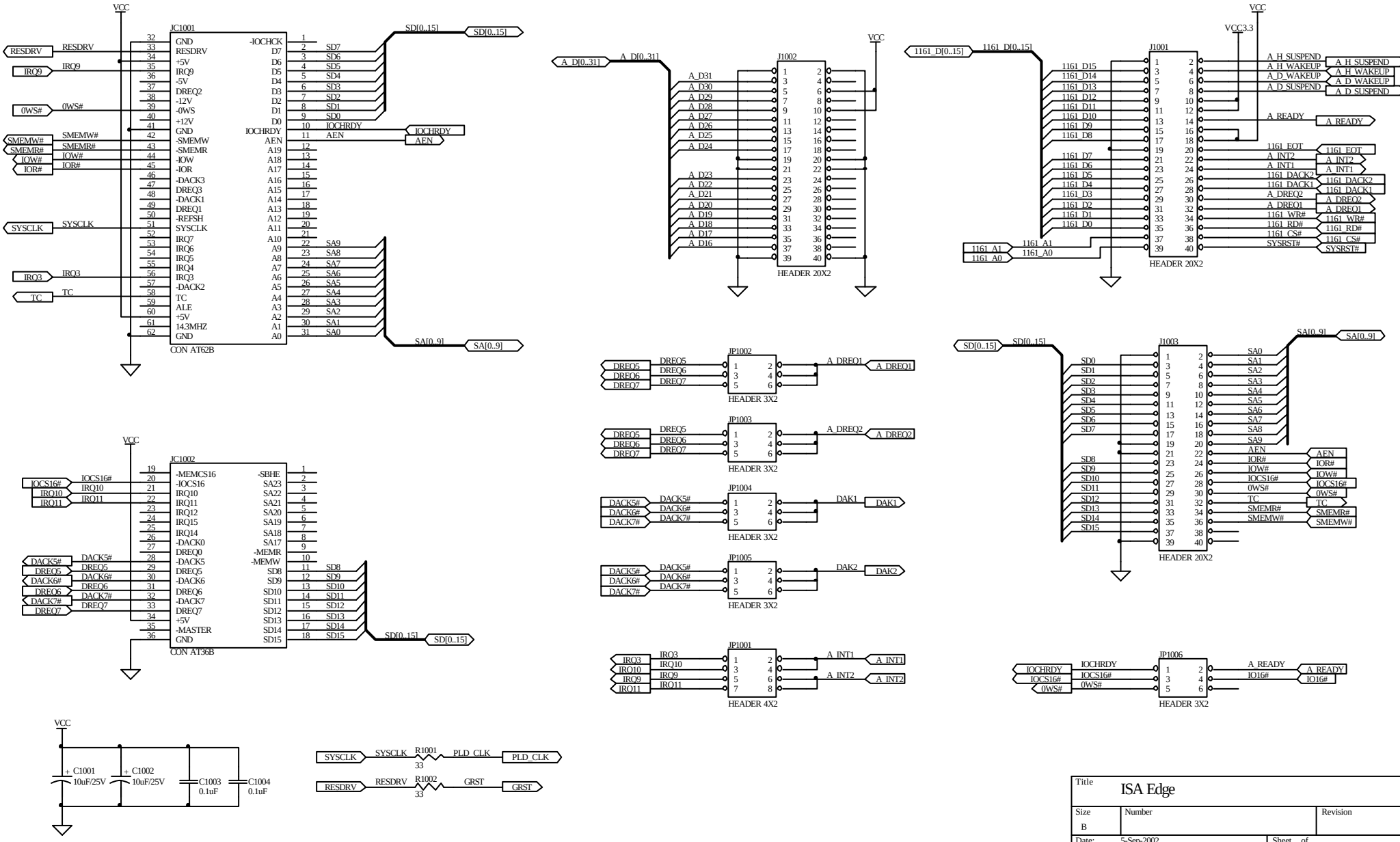
JC1001
CON AT62B
JC1002
CON AT36B
J1002
HEADER 20X2
J1001
HEADER 20X2
J1003
HEADER 20X2
JP1002
JP1003
JP1004
JP1005
JP1001
JP1006
HEADER 3X2
HEADER 4X2
VCC
VCC3.3
SD[0..15]
SA[0..9]
A_D[0..31]
1161_D[0..15]
R1001
R1002
33
C1001
10uF/25V
C1002
10uF/25V
C1003
0.1uF
C1004
0.1uF
SYSCLK
PLD_CLK
RESDRV
GRST
Title
ISA Edge
Size
B
Number
Revision
Date:
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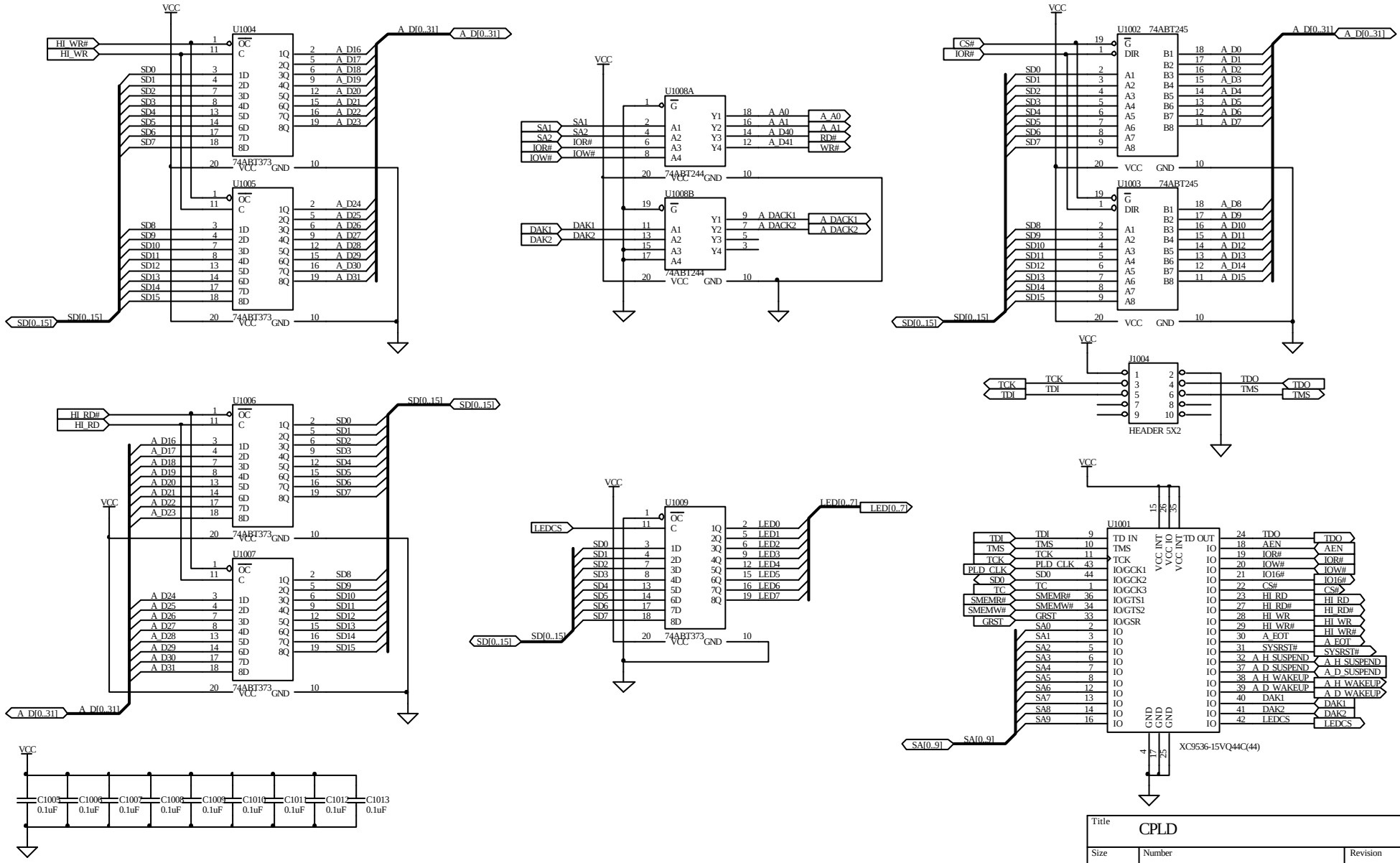

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Appendix B. References

- *ISP1160 Embedded Universal Serial Bus Host Controller* datasheet
- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1160 Embedded Programming Guide.*